

Code	Beeps	POST Routine Description
3Ch	2-1-2-3	Advanced configuration of chipset registers
3Dh		Load alternate registers with CMOS values
42h		Initialize interrupt vectors
45h		POST device initialization
46h		Check ROM copyright notice
48h		Check video configuration against CMOS
49h		Initialize PCI bus and devices
4Ah		Initialize all video adapters in system
4Bh		QuietBoot start (optional)
4Ch		Shadow video BIOS ROM
4Eh	2-2-3-1	Display BIOS copyright notice
50h		Display CPU type and speed
51h		Initialize EISA board
52h		Test keyboard
54h		Set key click if enabled
58h		Test for unexpected interrupts
59h		Initialize POST display service
5Ah		Display prompt Press F2 to enter SETUP
5Bh		Disable CPU cache
5Ch		Test RAM between 512 and 640 KB
60h	Electro help	Test extended memory
62h		Test extended memory address lines
64h		Jump to UserPatch1
66h		Configure advanced cache registers
67h		Initialize Multi Processor APIC
68h		Enable external and CPU caches
69h		Setup System Management Mode (SMM) area
6Ah		Display external L2 cache size
6Bh		Load custom defaults (optional)
6Ch		Display shadow-area message
6Eh		Display possible high address for UMB recovery
70h		Display error messages
72h		Check for configuration errors
76h		Check for keyboard errors
7Ch		Set up hardware interrupt vectors
7Eh		Initialize coprocessor if present
80h		Disable onboard Super I/O ports and IRQs
81h		Late POST device initialization
82h		Detect and install external RS232 ports
83h		Configure non-MCD IDE controllers
84h		Detect and install external parallel ports
85h		Initialize PC-compatible PnP ISA devices
86h		Re-initialize onboard I/O ports.

Acer Aspire One Beep Codes

J Dewey



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